

FIG. 1  
(PRIOR ART)

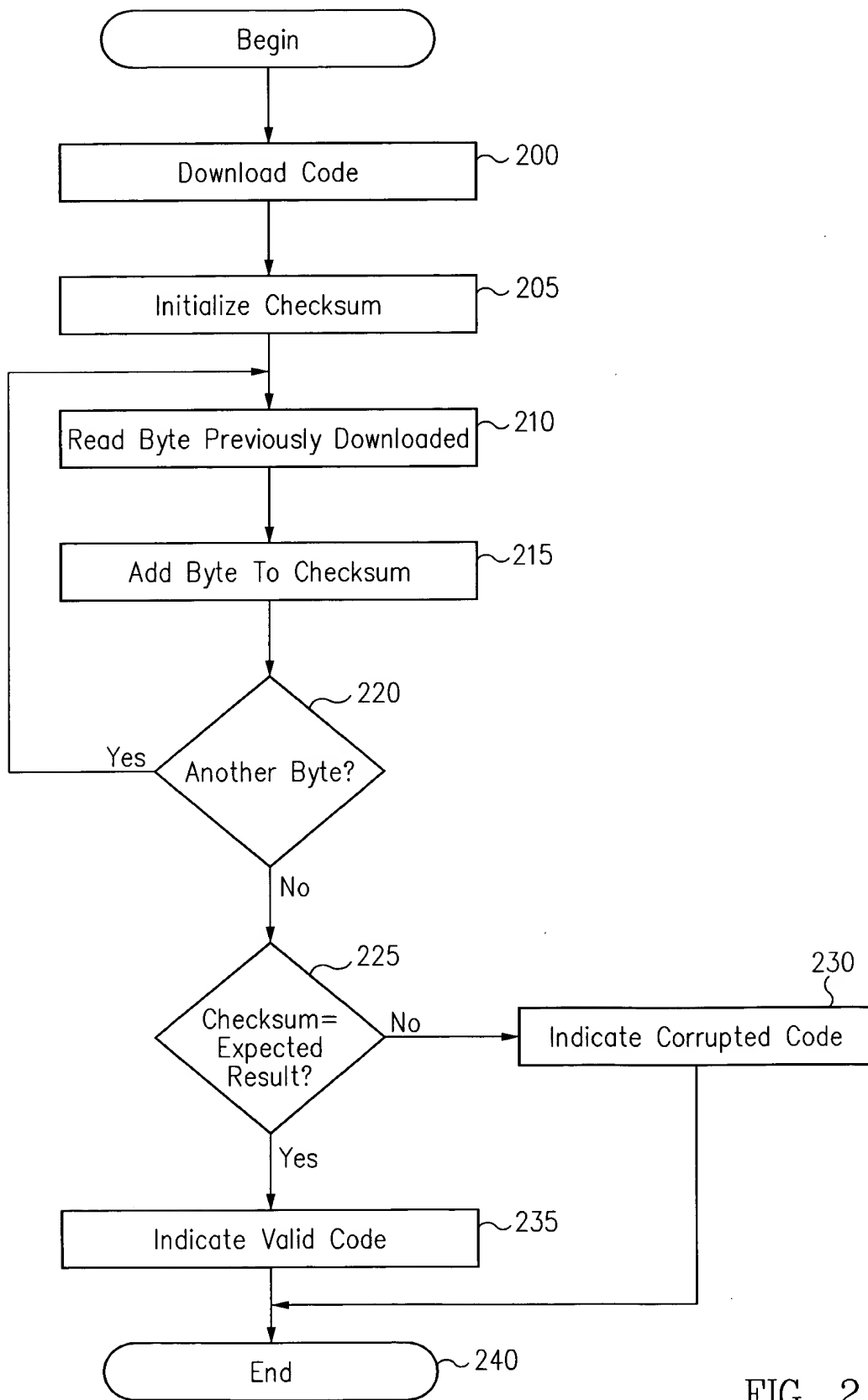


FIG. 2  
(PRIOR ART)

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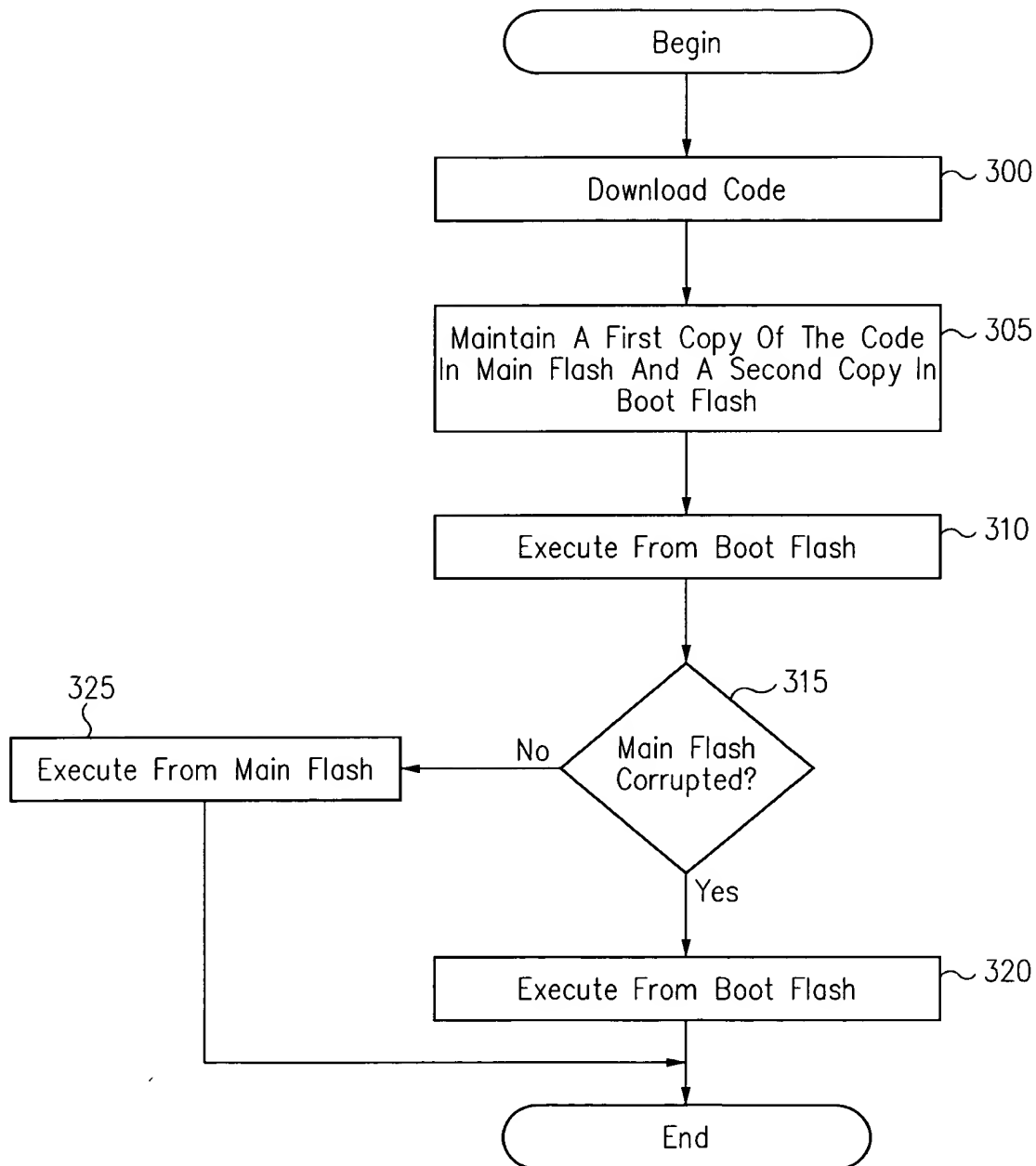


FIG. 3  
(PRIOR ART)

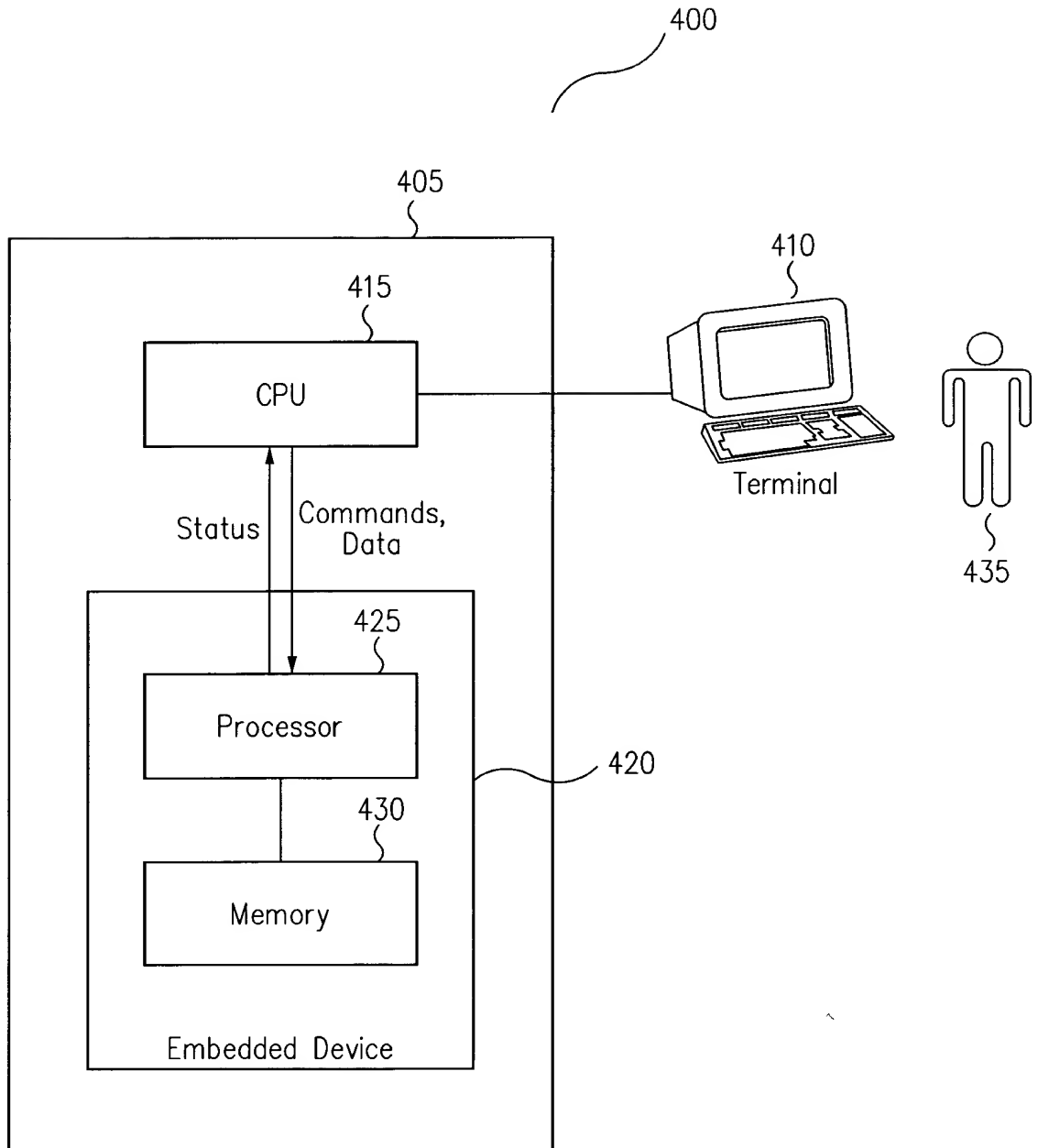


FIG. 4

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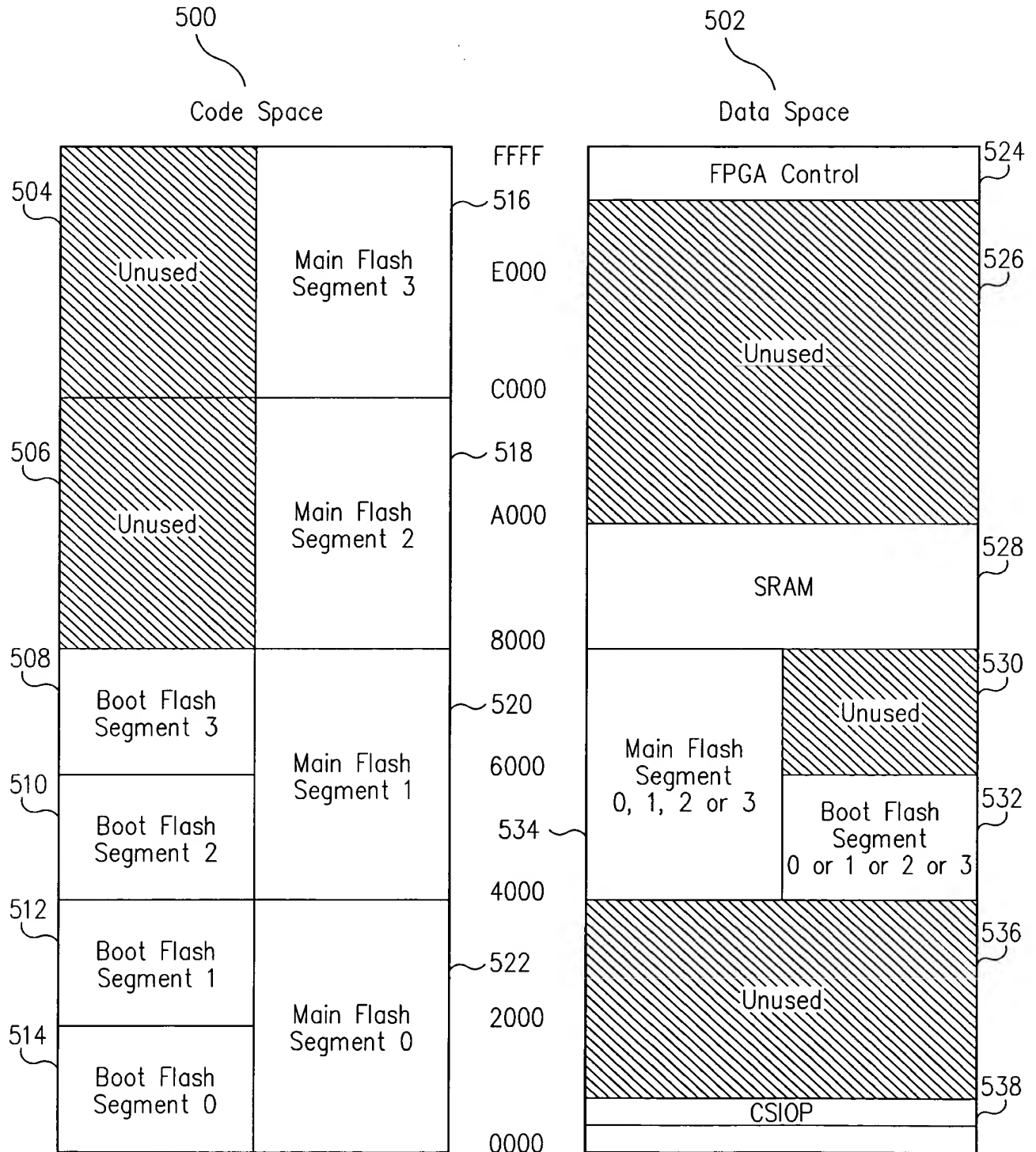


FIG. 5



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600

Page Register

Bit	Data	Note
605 0..2	Main Flash Segment Select	8 Segments Total
610 3..4	Boot Flash Segment Select	4 Segments Total
615 5	Flash Code Select	1: Main Flash Code 0: Boot Flash Code
620 6..7	Unused	

FIG. 6A

625

VM Register

Bit	Data
630 0	SRAM Is Code
635 1	Boot Flash Is Code
640 2	Main Flash Is Code
645 3	Boot Flash Is Data
650 4	Main Flash Is Data
655 5..6	Unused
660 7	Enable PIO

FIG. 6B



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700

Main Flash Segment 0 = (Device Space=Code) & (Flash Code Select=Main) & (address in 0000..3FFF)  
OR (Device Space=Data) & (Main Flash Segment Select=0) & (address in 4000..7FFF))  
Main Flash Segment 1 = (Device Space=Code) & (Flash Code Select=Main) & (address in 4000..7FFF)  
OR (Device Space=Data) & (Main Flash Segment Select=1) & (address in 4000..7FFF))  
Main Flash Segment 2 = (Device Space=Code) & (Flash Code Select=Main) & (address in 8000..BFFF)  
OR (Device Space=Data) & (Main Flash Segment Select=2) & (address in 4000..7FFF))  
Main Flash Segment 3 = (Device Space=Code) & (Flash Code Select=Main) & (address in C000..FFFF)  
OR (Device Space=Data) & (Main Flash Segment Select=3) & (address in 4000..7FFF))

FIG. 7A

705

Boot Flash Segment 0 = (Device Space=Code) & (Flash Code Select=Boot) & (address in 0000..1FFF)  
OR (Device Space=Data) & (Boot Flash Segment Select=0) & (address in 4000..5FFF))  
Boot Flash Segment 1 = (Device Space=Code) & (Flash Code Select=Boot) & (address in 2000..3FFF)  
OR (Device Space=Data) & (Boot Flash Segment Select=1) & (address in 4000..5FFF))  
Boot Flash Segment 2 = (Device Space=Code) & (Flash Code Select=Boot) & (address in 4000..5FFF)  
OR (Device Space=Data) & (Boot Flash Segment Select=2) & (address in 4000..5FFF))  
Boot Flash Segment 3 = (Device Space=Code) & (Flash Code Select=Boot) & (address in 6000..7FFF)  
OR (Device Space=Data) & (Boot Flash Segment Select=3) & (address in 4000..5FFF))

FIG. 7B



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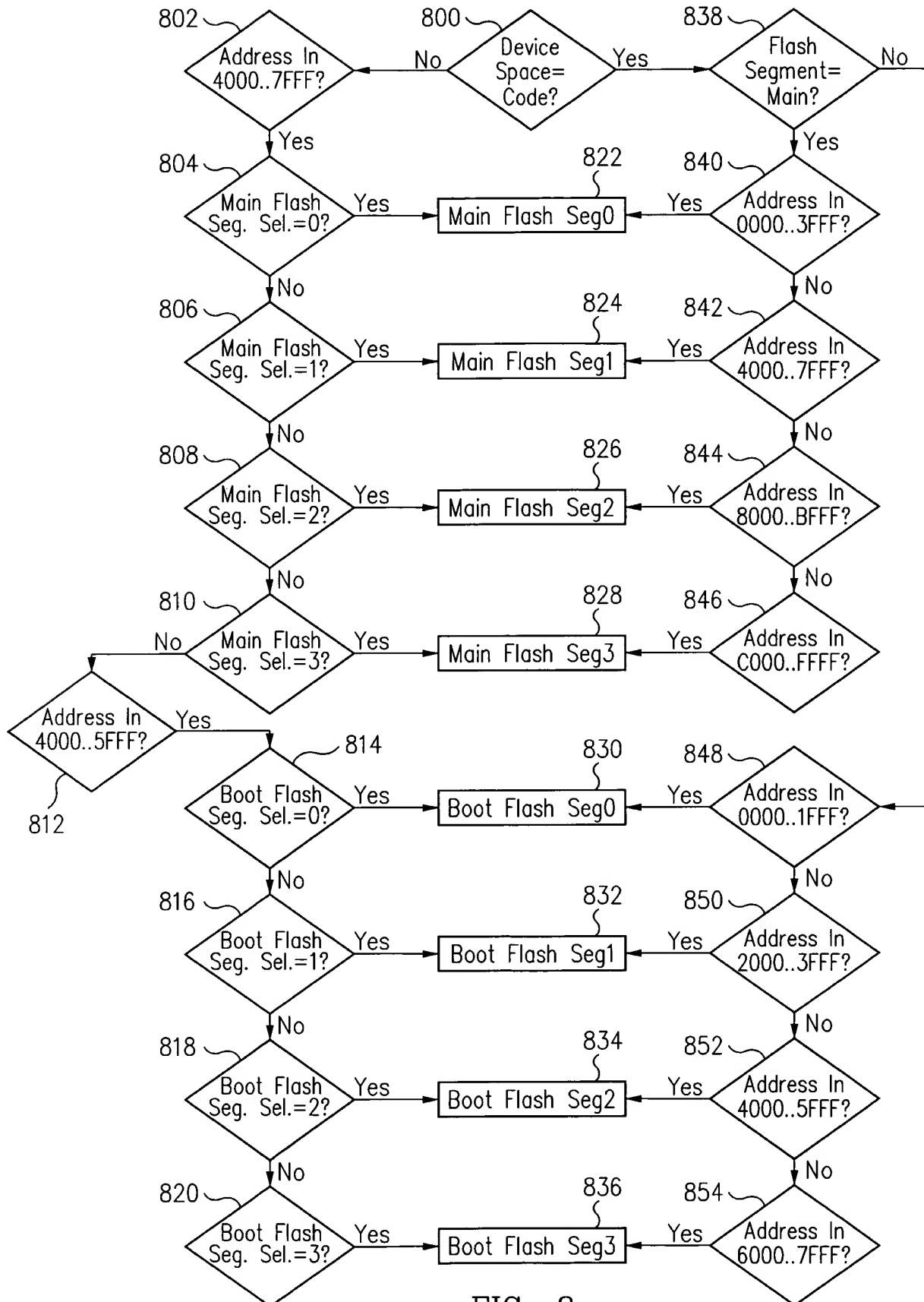


FIG. 8





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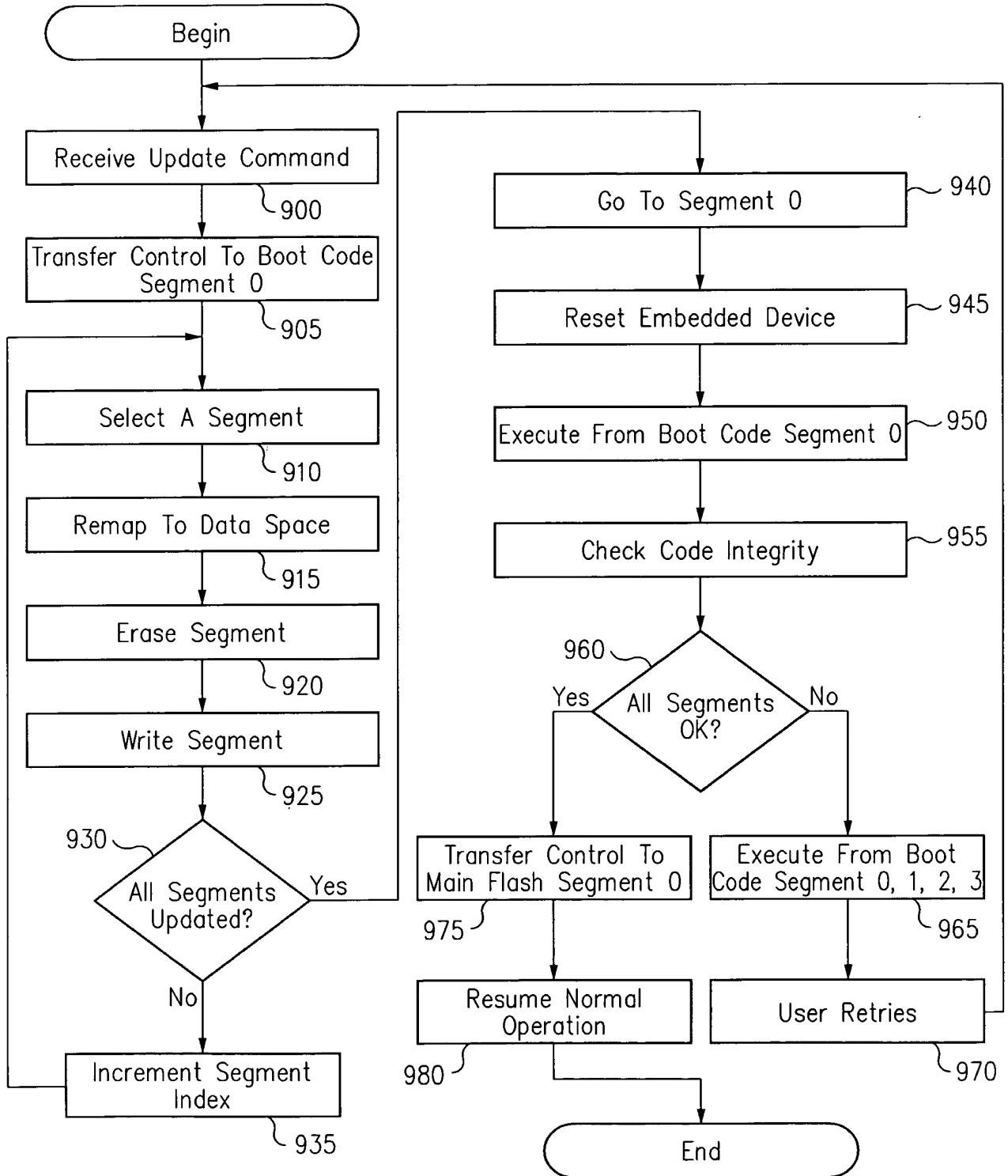


FIG. 9



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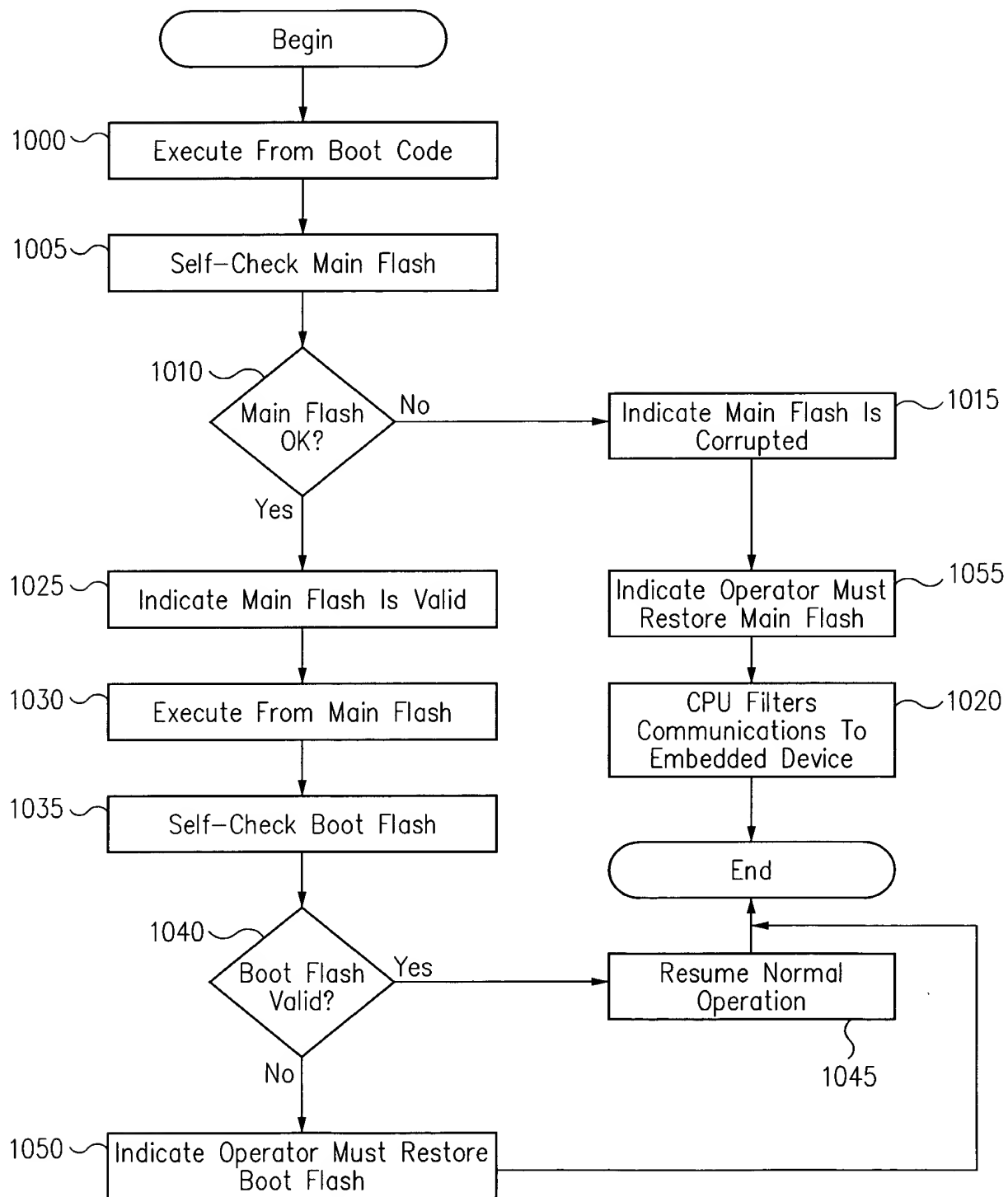


FIG. 10



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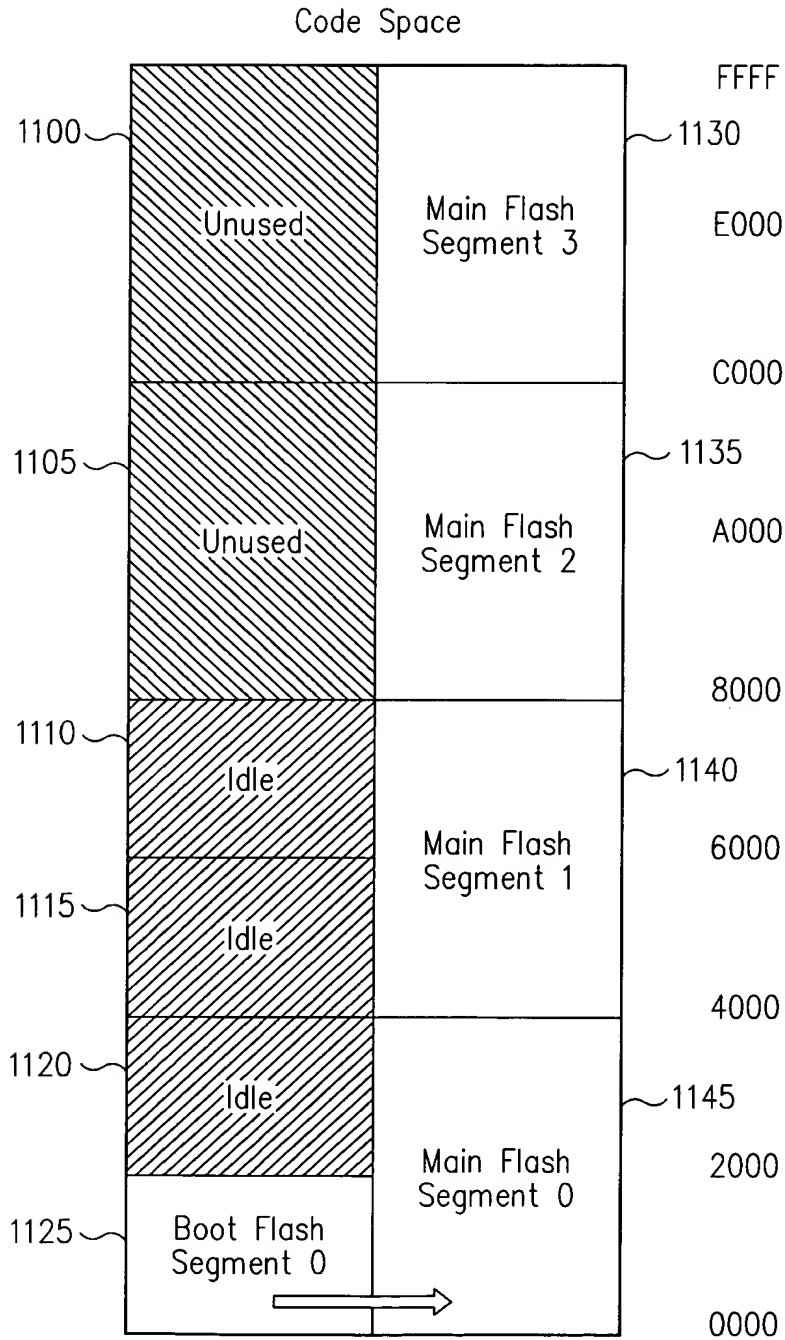


FIG. 11



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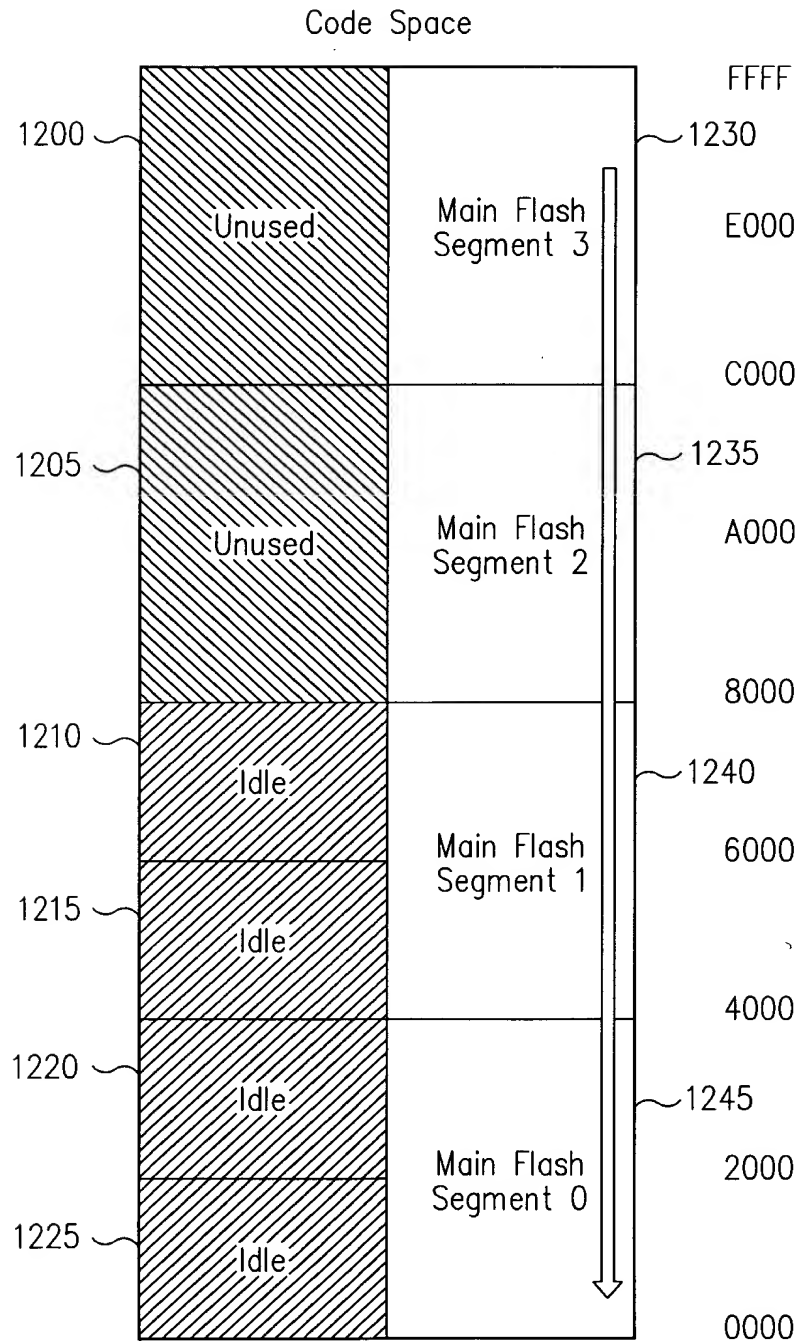


FIG. 12

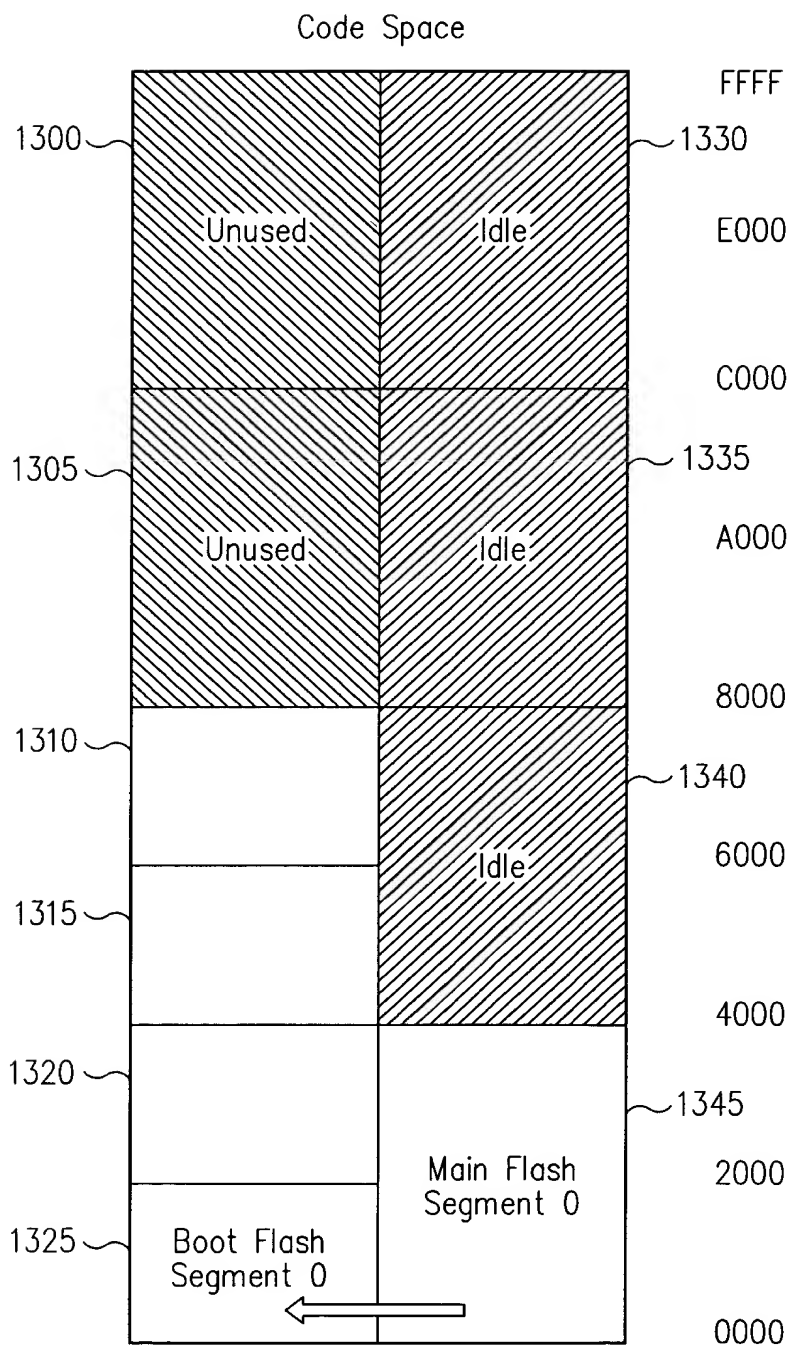


FIG. 13

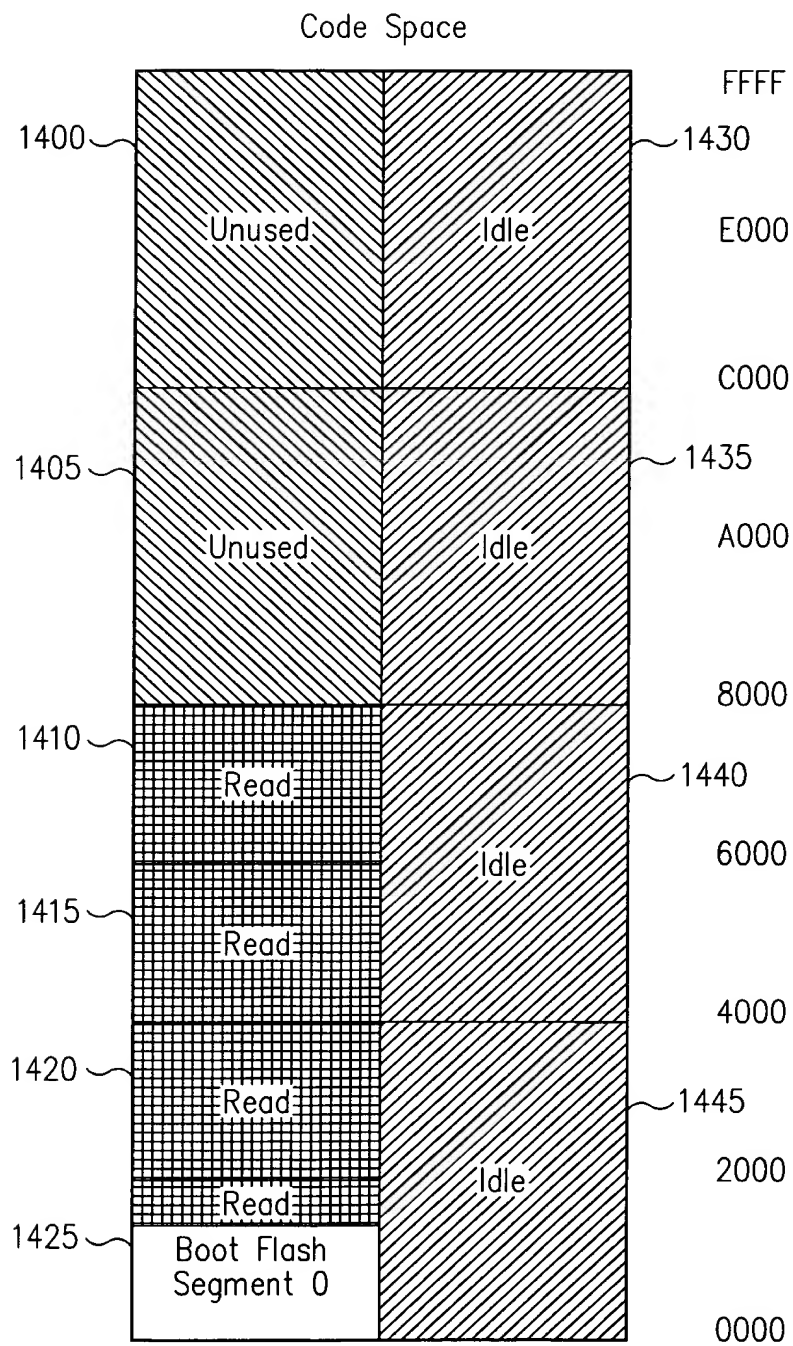
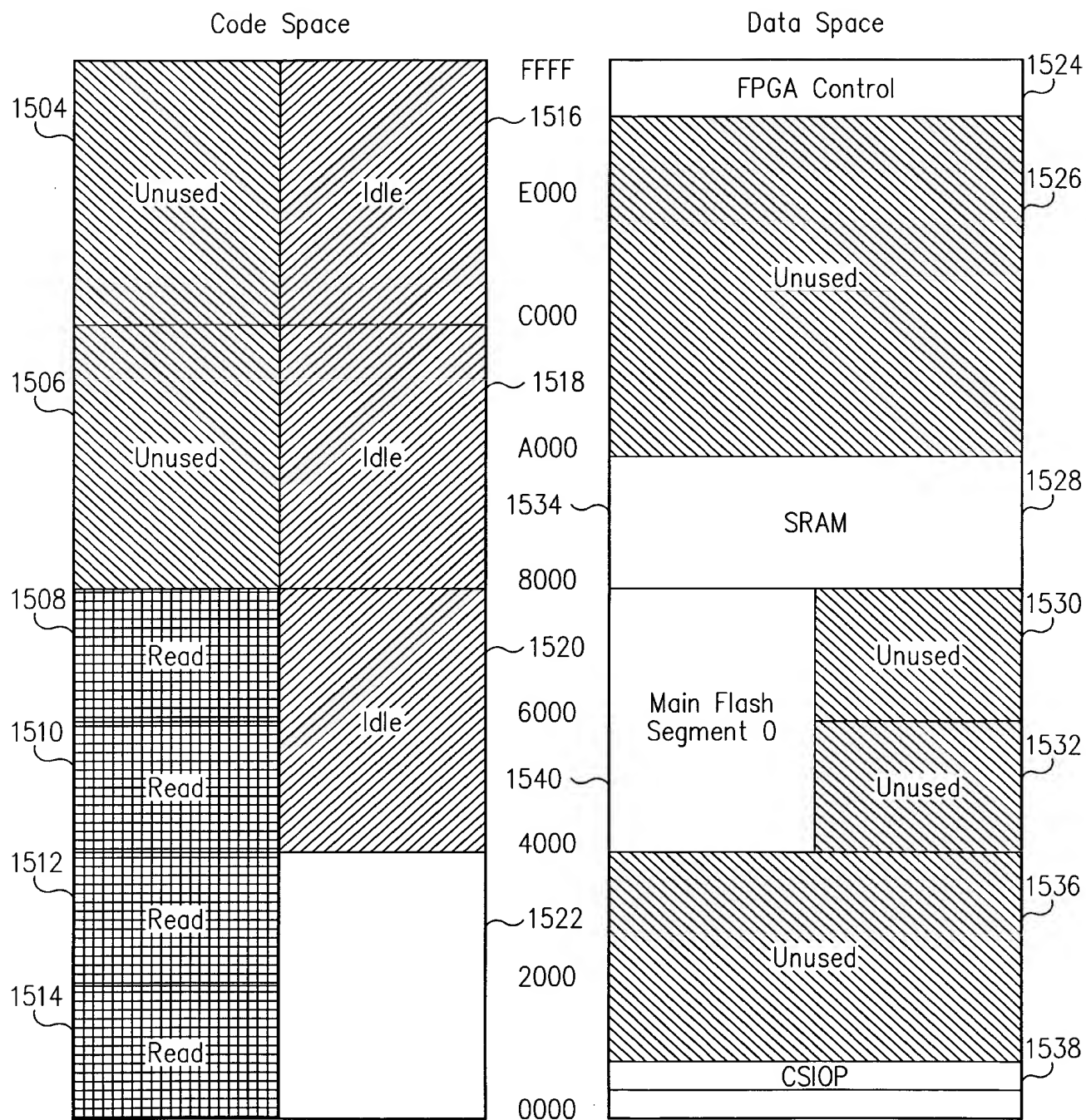


FIG. 14



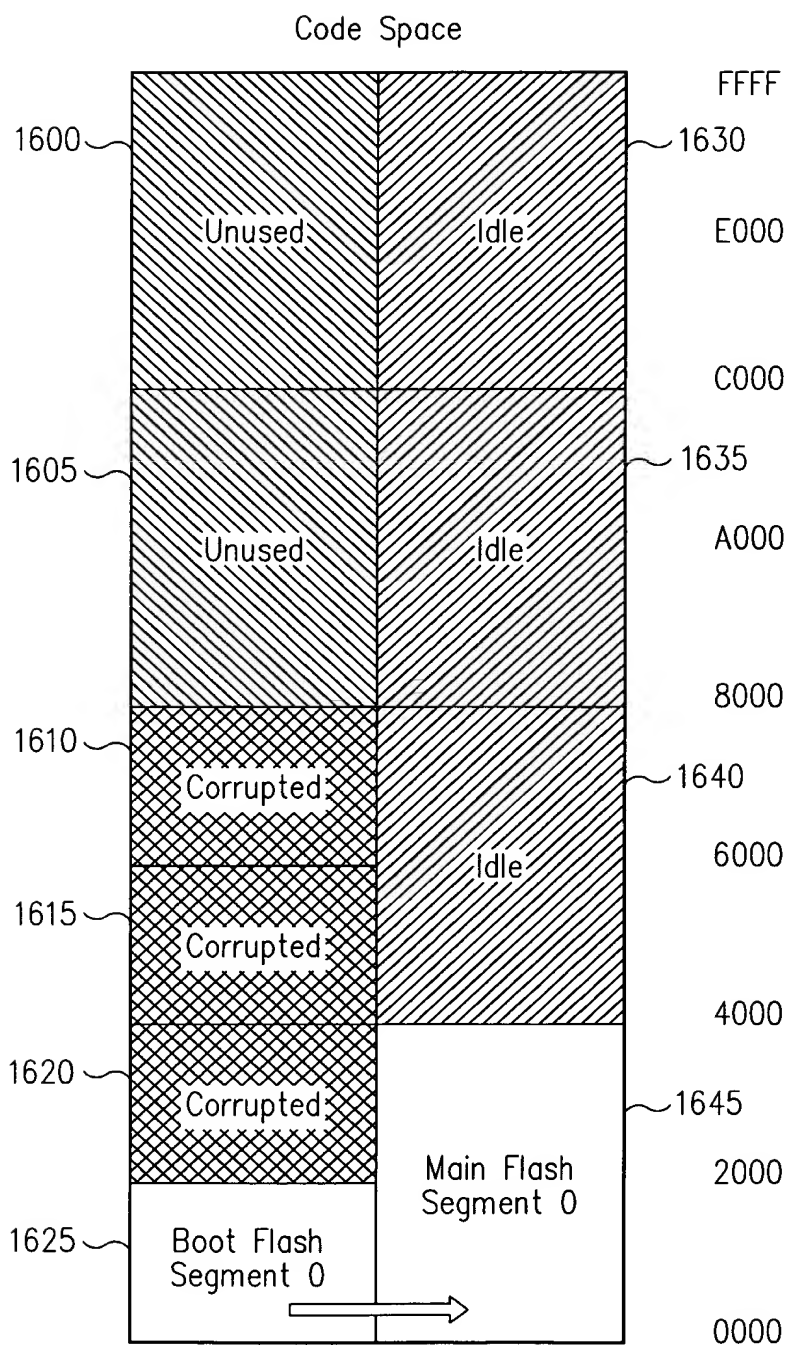


FIG. 16



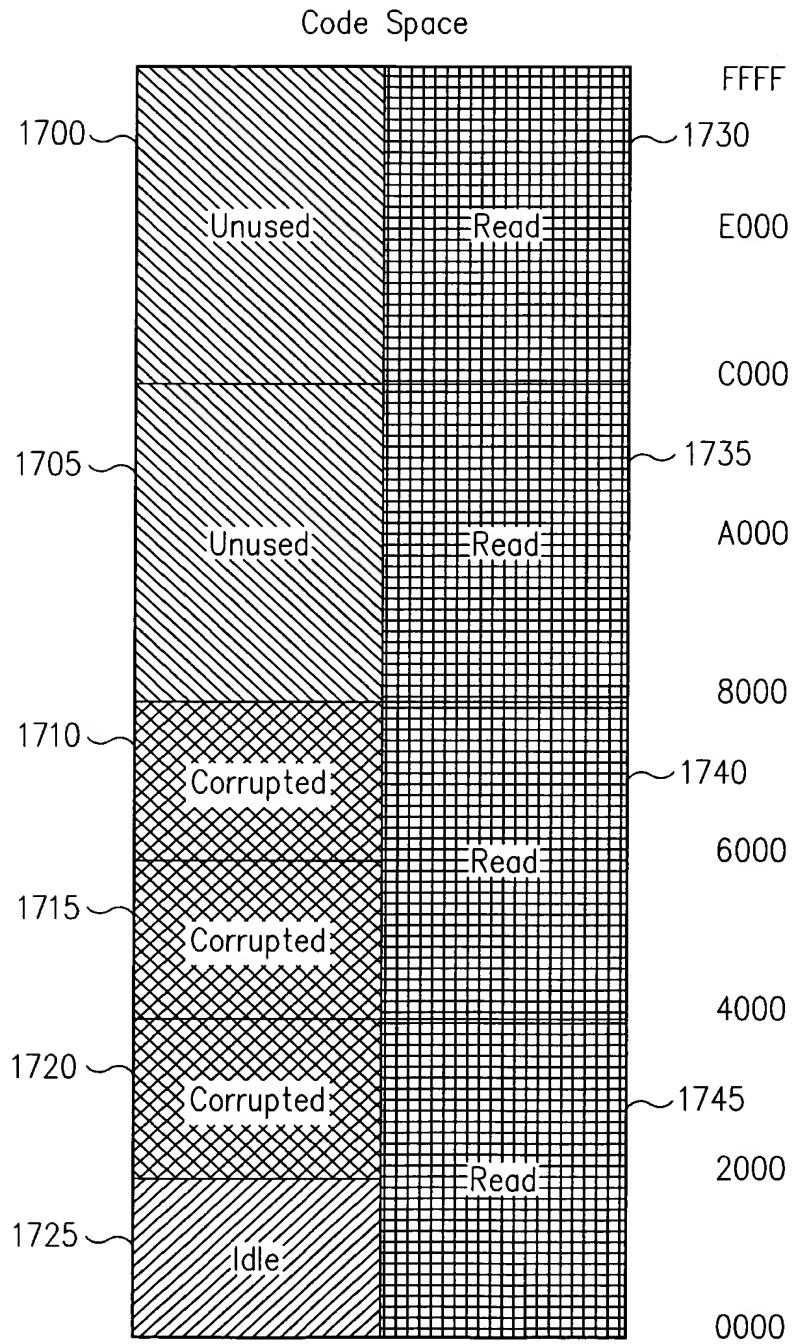


FIG. 17

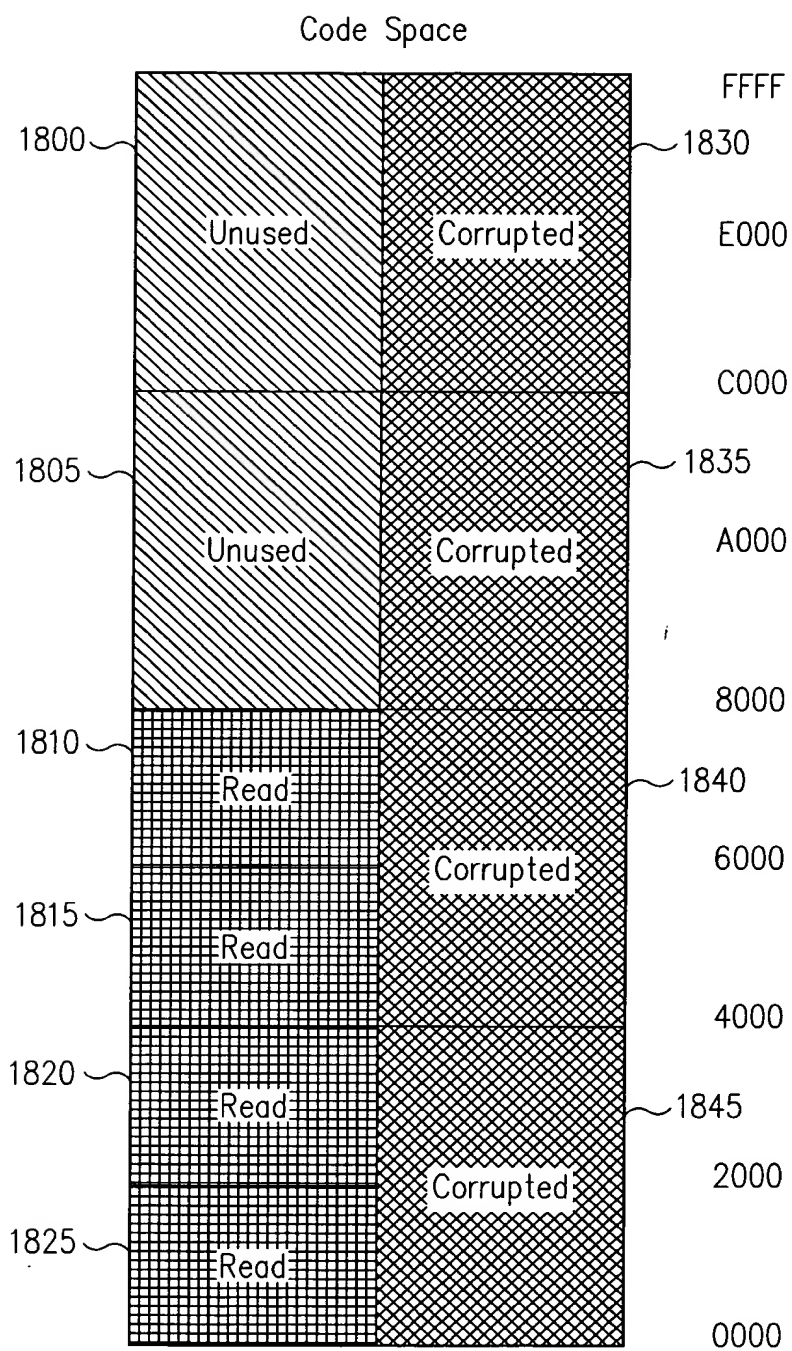


FIG. 18



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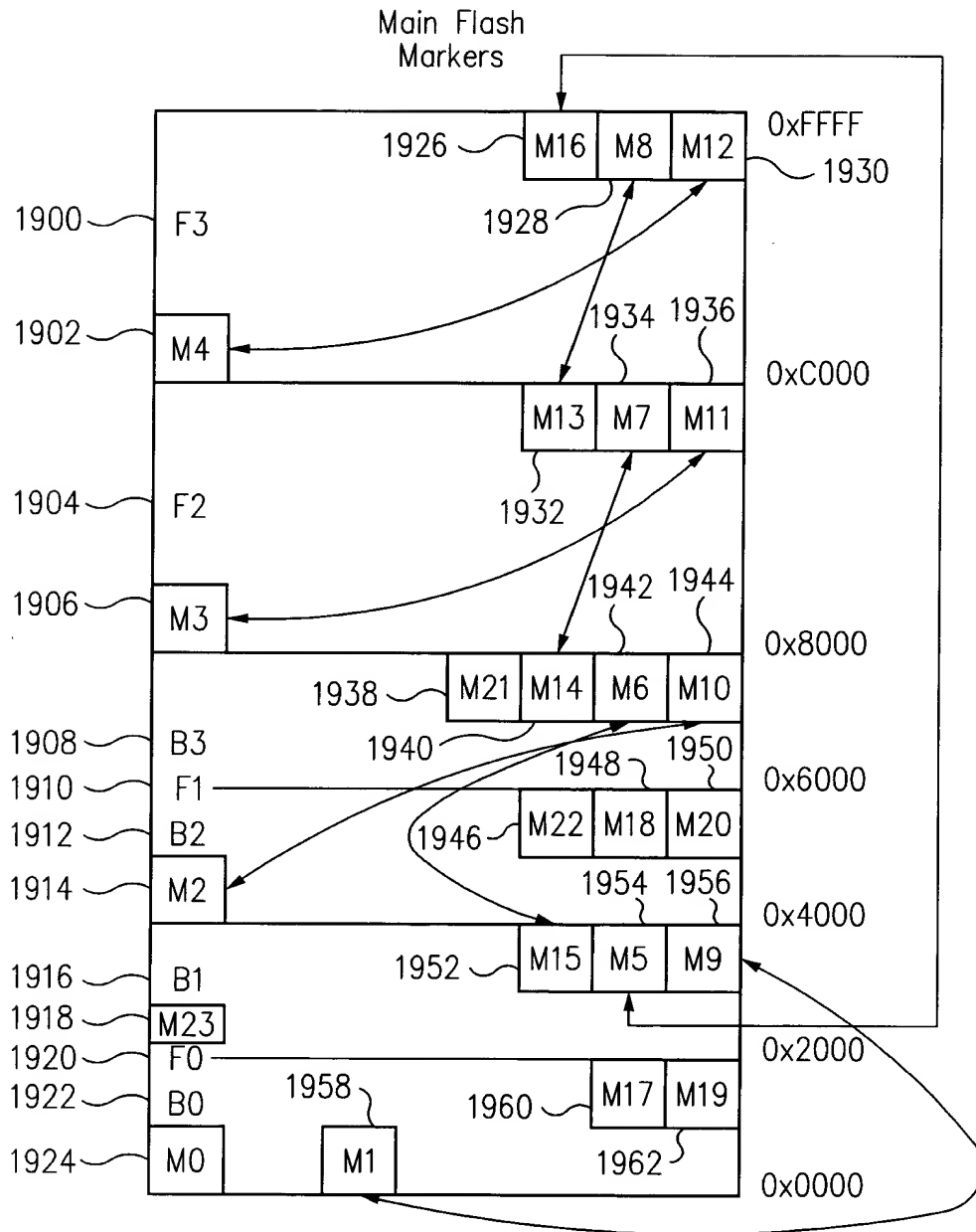


FIG. 19



Boot Flash  
Markers

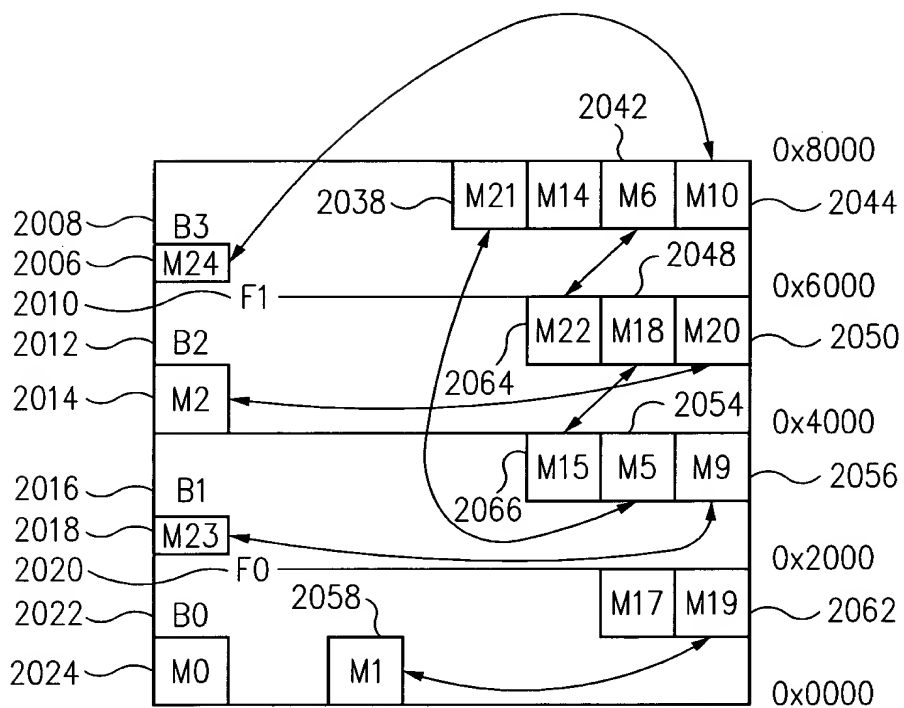


FIG. 20



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Marker  
Correlation

M	~M	
M4	M12	2100
M3	M11	
M2	M10	
M1	M9	
M8	M13	2105
M7	M14	
M6	M15	
M5	M16	

FIG. 21A

M	~M	
M24	M10	2110
M2	M20	
M23	M9	
M1	M19	
M5	M21	2115
M18	M15	
M6	M22	

FIG. 21B

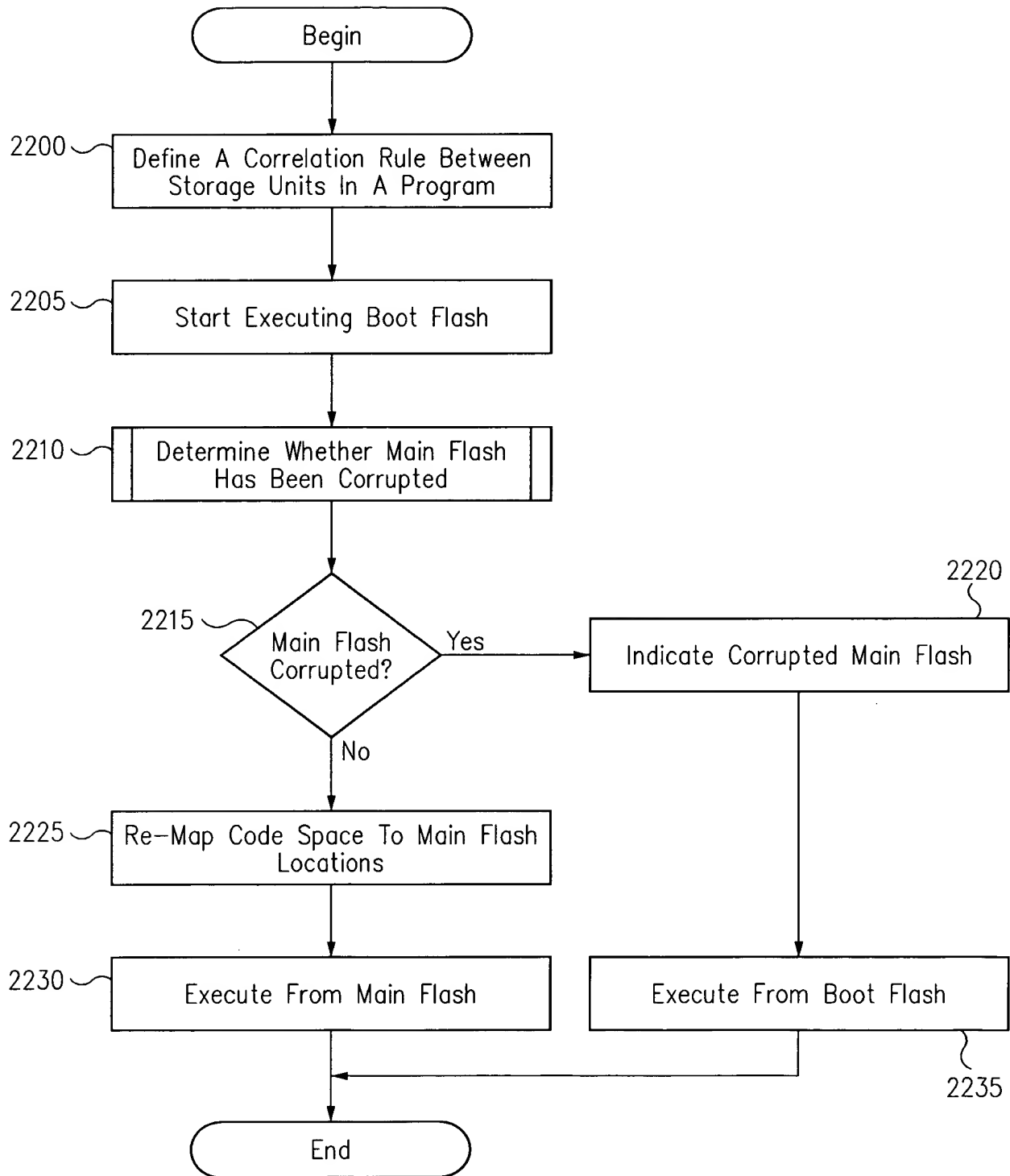


FIG. 22

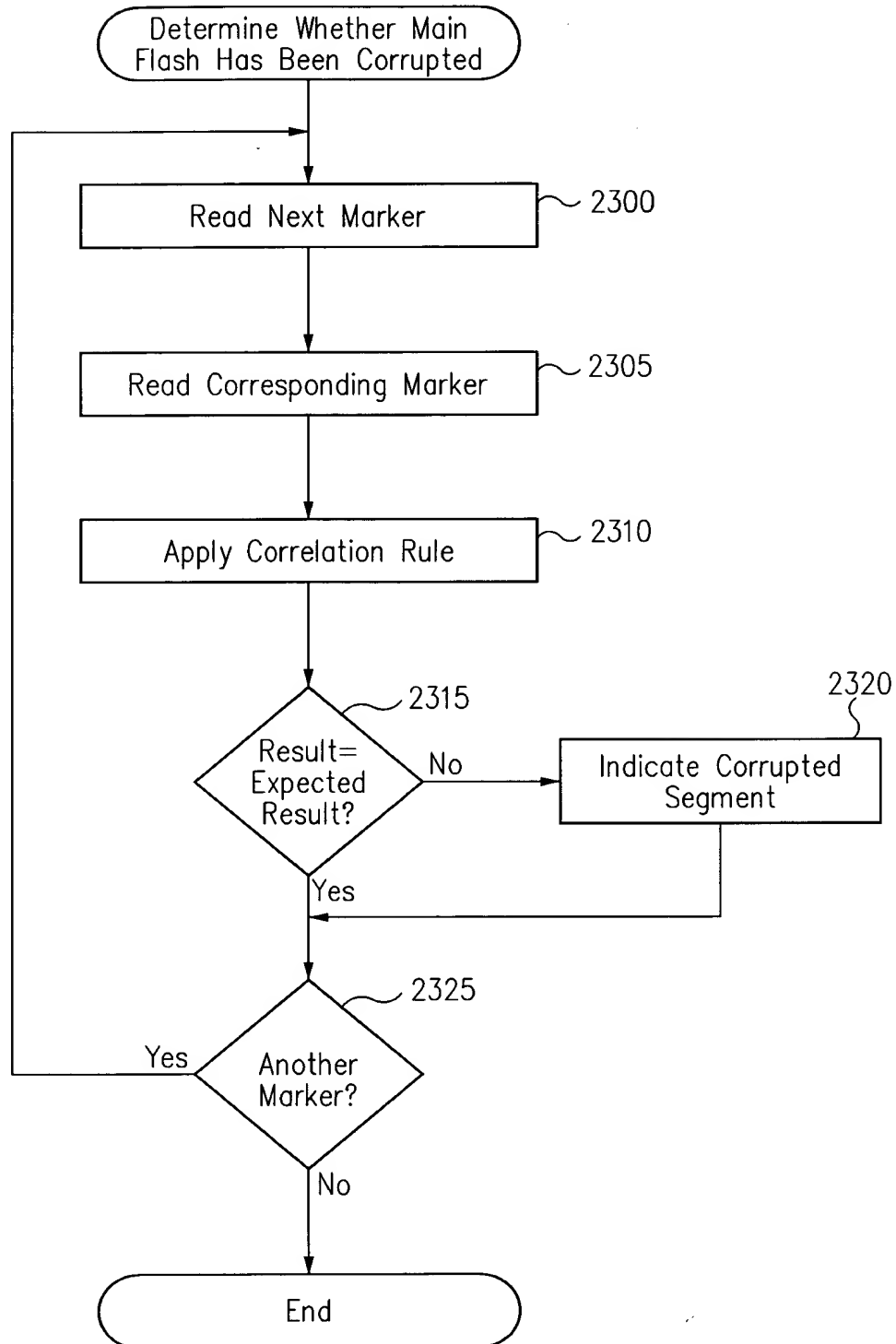


FIG. 23